Bit Error Location Analyzer (PELA2CHA)

BitWise Laboratories Bit Error Location Analyzer

Key Features

- Compact 2-Channel Error Detector
- 1-28 Gbps per Channel
- PRBS and User Patterns
- BER and Error Location Analysis
- Independent Delay and Threshold
- Shared Clock Input with Independent Channel Delay
- Single-ended or Differential Data
- Auxiliary Triggers
- Flexible Pattern Synchronization Including Two Channel Multiplexing Back to Single PRBS

Applications

- BER Testing in PAM4 or NRZ
- Burst Length
- Pattern Sensitivity
- FEC T-Strength Effectiveness
- Data Pattern Wander and Run-Length Histogram

BitWise Laboratories Bit Error Location Analyzer measures BER and error location statistics in up to two synchronous NRZ data streams at data rates from 1-28 Gbps. Signal interfacing is aided by flexible timing and threshold controls, auto pattern detection, simple quasi-eye diagrams, as well as support for a large number of true and inverted PRBS patterns and user-defined patterns. Special features support 2-channel multiplexing for MUX/DEMUX and PAM4 testing. This includes an automatic +/- 64-bit barrel shifting function to locate channel-to-channel synchronization in multiplexed 2-channel PRBS patterns.

Traditional BER testing is combined with error location analysis that records the precise bit location of each error in both streams. Individual channel and interleaved 2-channel analysis can be done simultaneously.

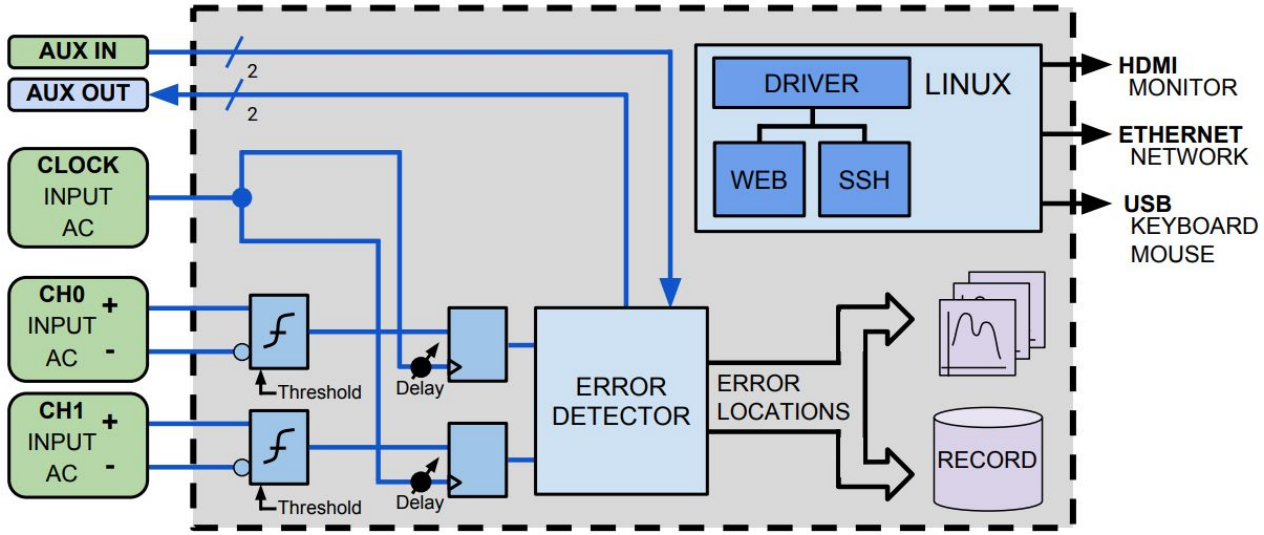
Error location analysis includes histograms of error-free intervals, burst error lengths, and error correlations to user-selectable modulo factors such as 204-byte FEC blocks or 127-bit patterns. More advanced analysis can display the amount of FEC correction strength (T-value) required to maintain error-free operation.

Incoming data can be captured and conveniently downloaded in ASCII format. Data pattern analysis allows you to measure run lengths and wander to a user-selectable window interval.

The user interface is served as a website from the device and is accessible from any desktop or mobile web browser. The device does not require connection to the Internet. Automation control is provided via TCP/IP socket interface using ASCII commands.

Web Browser User Interface

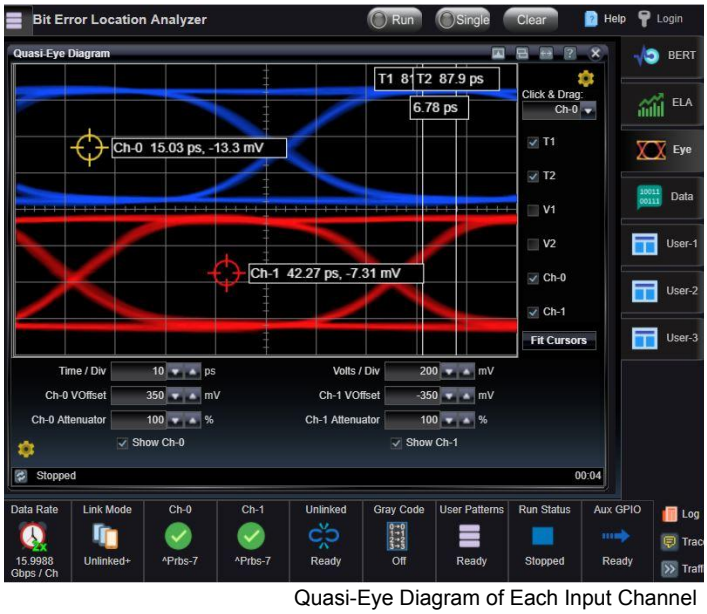
Basic BER measurements are displayed on individual and combined channels. A running strip-chart of error rates quickly shows relative performance over time. Status indicators along the bottom show the current operating status. On the right, the user can easily access other pages of analysis features.



Error Detector Block Diagram

Interfacing signals to the Bit Error Location Analyzer is done using the control settings dialogs available from the Status indicators located in the Status Bar at the bottom of the web browser user interface. Configuring the Bit Error Location Analyzer to accept either a full-rate or half-rate input clock is accomplished by accessing the Data Rate Settings dialog from the the "Data Rate" Status Bar indicator. Each channel can be configured for a variety of PRBS patterns or can be set to auto-search all available patterns. The Two channels can be independently synchronized for BER measurement, or they can be ***Linked*** *together requiring automatic bit interleave alignment and cross-channel synchronization.*

Basic ELA Statistics and Channel 1 Detector Settings



Quasi-Eye Diagram of Each Input Channel

The Eye Diagram feature shows individual channel eye openings and allows you to choose sampling time and voltage threshold for each channel. The Bit Error Location Analyzer also supports an "Auto-align" function that will automatically find good sample points. Or, you can click and drag the sample point icons to different locations. This Quasi-Eye Diagram display provides a quick check of your incoming signals to make sure everything is okay before making BER measurements.

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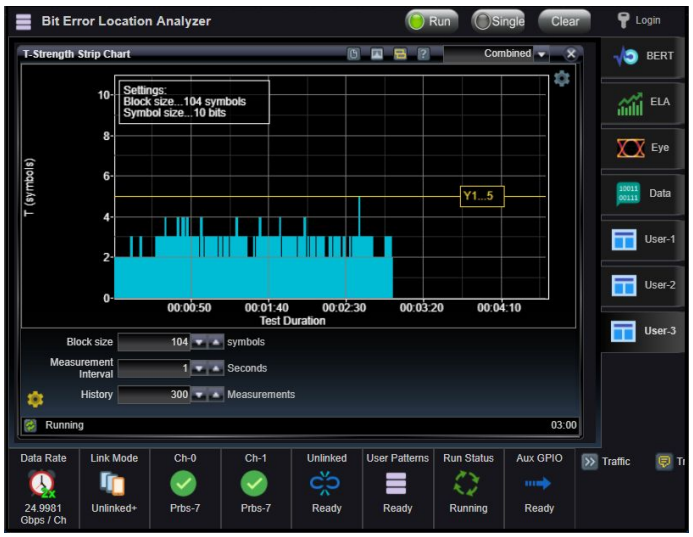


Block T-Value Strip Chart showing required FEC strength

FEC block and symbol sizes can be configured to perform error analysis for specific block-code FEC architectures. By grouping consecutive bit errors into symbol errors, the Bit Error Location Analyzer can report symbol-oriented correction strength "T" required to correct all errors during specified test intervals.

The Bit Error Location Analyzer displays bit error counts and error rates for the individual MSB and LSB channels as well as for the combined Interleaved stream. Synchronization is constantly checked and displayed in the channel Status Bar indicators. The synchronization mechanism can be configured to attempt resynchronization if large error events are encountered to minimize interruption.

The ELA Error Free Histogram is an advanced error location analysis technique that shows the distribution of error-free intervals during a test session. Any interval between errors that more likely to happen defines a systematic error source. The length of the interval is diagnostic and helps to identify the source condition. For example, if a 25 Gbps system tended to have error-free intervals of 250,000 bits (or octaves of this), then errors would be happening at 100 KHz, and debugging would need to consider what system components had any interaction with 100 KHz - A likely candidate might be a switching power supply.

Error correlations can be precisely checked using the ELA Modulo Histogram. By configuring the histogram to show entries modulo the length of the data pattern, errors that are correlated with the pattern bit sequence are easy to see. These types of pattern-sensitive errors are often caused by Inter-symbol Interference (ISI).

Application Note: PAM4 BER TESTING

In PAM4 applications, a common test methodology for Error Detection is to perform clock recovery on the PAM4 signal and to separate the 4-Level PAM4 signal into two NRZ streams representing the MSB and LSB channels, and to test each of the two channels using BER analysis.

These signals are provided to the Bit Error Location Analyzer (PELA2CHA) that accepts two NRZ data streams and one clock. Sampling points for the two NRZ streams are selected by performing an Auto-align function,or by manually choosing sample locations on the built-in Quasi-Eye diagram display. Setting the LinkMode to *Interleaved* mode enables synchronization and error analysis as if the two channels of incoming data were from a single PRBS stream bit de-interleaved into the MSB and LSB channels of the PAM4 signal.

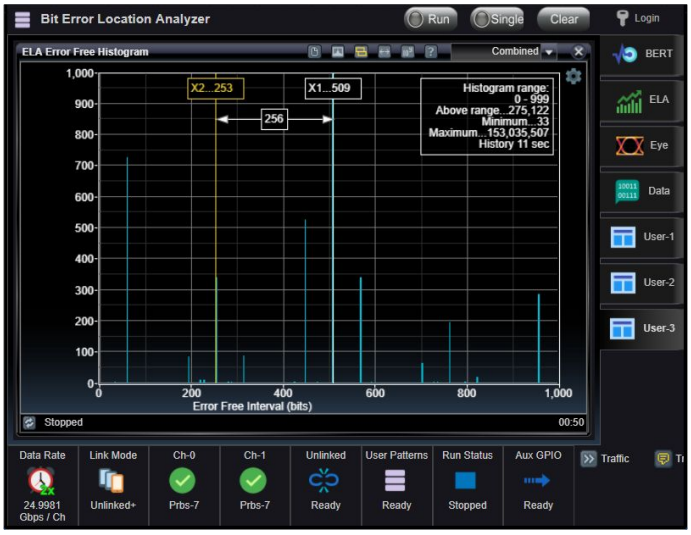
Once configured, the front panel of the Bit Error Location Analyzer displays green LEDs indicating pattern synchronization that means you're ready to make BER measurements.

Correlation modulo-127 Analysis showing Pattern Sensitivity

The ELA Modulo Histogram shows the number of errors detected at each bit position of a the 127-bit repeating PRBS7 pattern during a short duration of testing. You can see that not all bits of the pattern had the same probability of error. In fact two spots were predominantly responsible for errors which demonstrates error pattern sensitivity that can be a signature of Inter-symbol Interference (ISI) impacts on performance. This is a good example of how Error Location Analysis is used to diagnose the cause of bit errors.

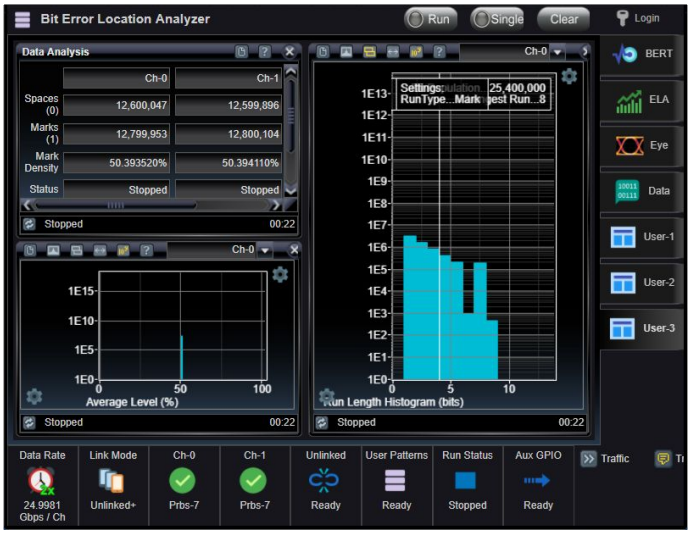
Block T-Value Strip Chart showing required FEC strength

The ELA Block Error Histogram provides for defining a system Symbol Size (in bits) and Block Size (in symbols) and subsequently to histogram the number of errored symbols per block during the test session. This type of information is critical when designing error management strategies such as CRC error detection and block-based forward error correction systems since it informs the requirement for how much correction strength is necessary.



Input data Run Length Histogram

The ELA Error Free histogram demonstrates if some error-free intervals are more likely than others. This implies systematic, non-random error sources. In this example, the systematic errors are also harmonically related because they occur at a common spacing. This is a great clue to identify the source of bit error problems.



Input data Run Length Histogram

Mark/Space Density and data pattern wander is another critical data pattern characteristic that affects AC-coupled and/or DC-restored communications and clock recovery systems. The Data Wander and Data Run Length analyses captures 4 Mbit segments of user data and continuously computes running variations of wander and run lengths. This example shows a Run Length histogram for a channel using PRBS7 data with a small background bit error rate. The small population of 6- and 8-bit run lengths are due to the background error rate since these run lengths are not present in an error-free PRBS7 pattern. The example also shows that Mark Density and Data Wander for such a short pattern is highly consistent.

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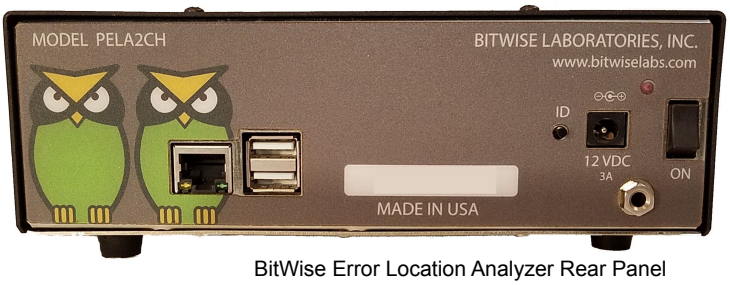
Performance

Data Rate	*1-28 Gbps per channel, synchronous*
BER Measurements	*Individual and combined bits, errors, BER (Bit Error Ratio),*
Error Location Analysis	*SER (Symbol Error Ratio), Block Histogram, Burst Histogram, Correlation Histogram, Error-Free Histogram, T-value Strip Chart*
User Data Analysis	*Run-Length, Mark Density, Wander (with adjustable bit window)*
Variable Delay	*0-140 psec (0.1 ps resolution) each channel*
Variable Threshold	*+/- 1000 mV from center*
Patterns	*4 Mbit or PRBSn (n=7,11,13,15,20,23,31)*
Input Data	*2.92 mm, Differential, AC-coupled*
Input Clock	*2.92 mm, Single-ended, AC-coupled*
Triggers	*Pattern sync, error flag (pulse stretched)*
Network	*10/100 Mb Ethernet, RJ45*
Power Supply	*100-240 VAC to 12 V, 5A, CE/FCC/UL Certified*
Power	*22 watt (typical)*
Dimensions	*6" (L) x 7-1/2" (W) x 2-1/2" (H)*

Warranty

Products from BitWise Laboratories. come with a one year limited warranty. BitWise Laboratories will repair or, at its option, replace any defective product returned to BitWise Laboratories within one year of the date of purchase. This warranty applies to defects that are not due to misuse, neglect, accident or by abnormal operating conditions. Contact us for return material authorization. An additional 2-year warranty extension is available at the time of purchase.



BitWise Error Location Analyzer Rear Panel

Ordering Information

PELA2CHA	**Bit Error Location Analyzer**
WARRANTY2YR	**Additional 2 year warranty**

Send email requests to: sales@bitwiselabs.com

Company

BitWise Laboratories is located in California USA in the heart of Silicon Valley. Our founders have spent decades in Test & Measurement specializing in creating innovative tools that are easy to use and provide more diagnostic information for development and test engineering. The BitWise Laboratories line of products builds on this legacy and provides RF and PAM4 tools for today's communications engineering challenges. We provide compact and economical instruments that utilize world-class SiGe technology to achieve uncompromising performance. We provide innovative software with convenient multi-user web browser user interfaces for viewing and easy data download with complete remote control automation. And we listen to our customers to help us define the next generation of features that will make our tools even better.